**[ME11]**
**UKM8032 microcontroller design and FPGA implementation by integrating DW8051 IP core for SoC design**

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The project has successfully designed and implemented a high performance Intel compatible 8-bits 8032 microcontroller, using state-of-the-art Electronic Design Automation (EDA) tools from Cadence and Synopsys which have been widely used in Very Large Scale Integration (VLSI) design industry. These tools were used towards realizing a System-on-Chip (SoC) design, i.e. UKM8032 microcontroller system, which consists of DW8051 Intellectual Property (IP) core and some other subcomponents that were designed using IEEE 1364-1995 Verilog Hardware Description Language (HDL) as the environment for hardware design. Due to unavailability of the ASIC technology library, an Application Specific Integrated Circuit (ASIC) priori implementation of the UKM8032 has been developed and functionally verified at Register Transfer Level (RTL), before the design was migrated to Field Programmable Grid Array (FPGA) implementation which will be synthesized by Synopsys's Design Compiler (DC) with Xilinx's Virtex2 technology library. The integration of the DW8051 IP core and subcomponents such as 8-bits bidirectional input-output (I/O) ports, 256-bytes Random Access Memory (RAM) unit, and external Special Function Register (SFR) units to form a SoC microcontroller, was simulated to verify its functionality by using Synopsys's Verilog Compiler and Simulator (VCS). The verification result for every abstract level matches the required specification and functionality. Instead of extensive simulation on design's behaviour, an internal Read Only Memory (ROM) unit has been incorporated into the design for testing purposes. Simple programs have been developed and tested on real hardware utilizing as much instruction sets as possible and the design is able to reach operating speed up to 100MHz on Virtex2 FPGA board by using Integrated Synthesis Environment (ISE) software from Xilinx. The microcontroller has been successfully implemented in FPGA hardware that means it will have higher chance of success when presuming the ASIC implementation for fabrication in the future.